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IMPROVED SIGNAL ROUTING BETWEEN A MEMORY

CONTROL UNIT AND A MEMORY DEVICE

1/3



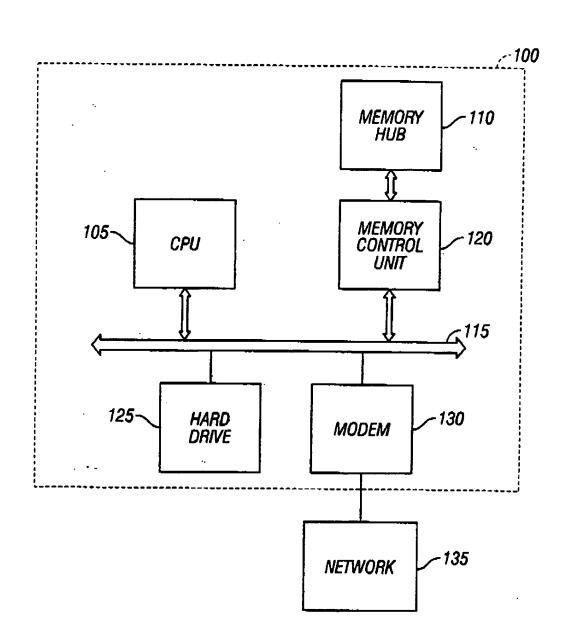


FIG. 1 (Prior Art)

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IMPROVED SIGNAL ROUTING BETWEEN A MEMORY

CONTROL UNIT AND A MEMORY DEVICE

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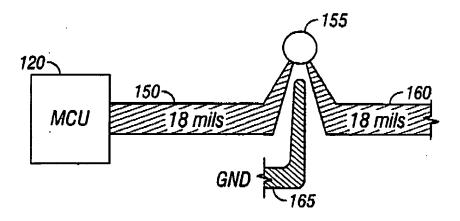
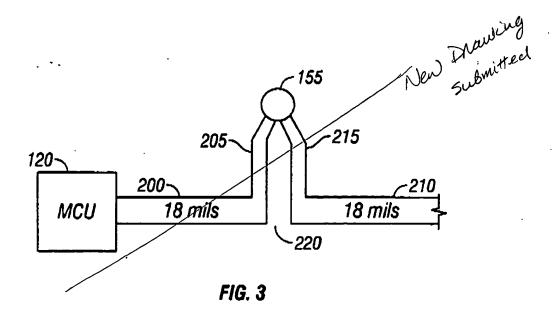


FIG. 2 (Prior Art)



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